CHAPTER 1

INTRODUCTION TO CMOS DACs

1.1 INTRODUCTION

This text is about CMOS D/A converters—particularly those based on an R-2R resistive ladder network. Since its introduction in 1973 this type of CMOS D/A converter has gained enormous popularity; the aim of this booklet is to explain the basic properties of the circuit and to show how it can best be applied. The emphasis is on the *applications* of CMOS D/A converters rather than the internal design of the circuit although, as always, it is necessary to understand something of the internal workings in order to get the most out of it.

1.2 A BASIC DAC

Most CMOS DACs are based on the circuit shown in Figure 1.1. An external reference is applied to the V_{REF} pin and the R-2R ladder divides the input current I into binary-weighted currents as shown. These currents are then steered by current steering switches to the OUT1 node or to the OUT2 node. The digital input to the D/A converter determines the position of the switch. A logic "1" causes the switch to steer the current to OUT1, a logic "0" causes the switch to steer the current to OUT2. Note that OUT2 is at ground. Feedback around the op

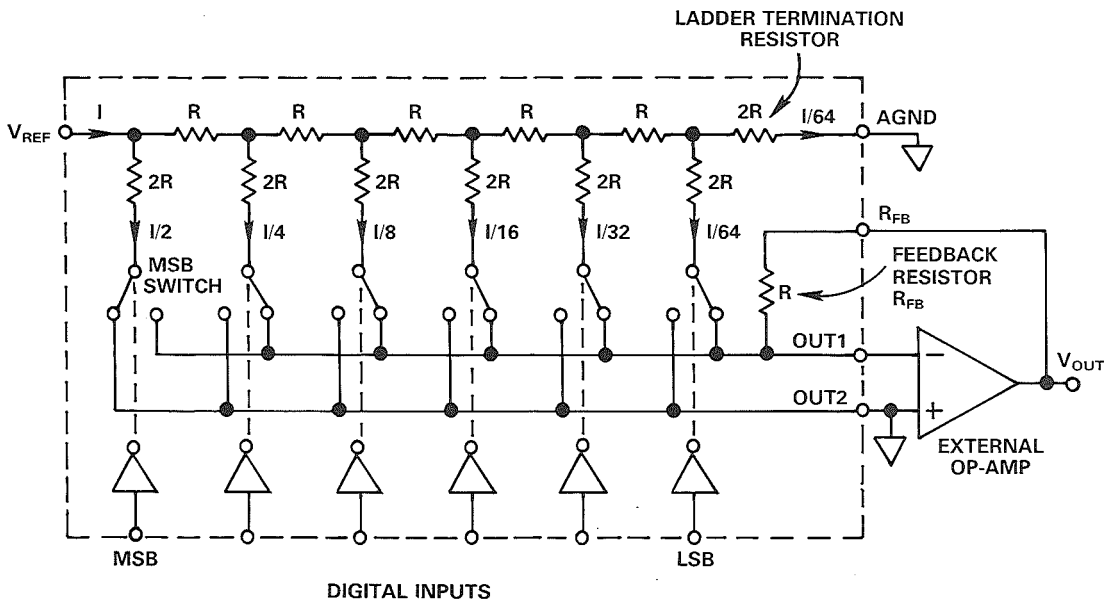

Figure 1.1 Simplified 6-Bit Current-Steering DAC

amp forces OUT1 to also be at ground potential. Thus both switch states look alike to the network. All "0's" at the input causes all the switchable currents to flow to OUT2, all "1's" causes all the switchable currents to flow to OUT1. In the six-bit DAC shown a digital input of "100000" causes I/2 to flow to OUT1 and the remainder of the current to OUT2, thus half the input current is available at OUT1 and 100000 corresponds to half scale. For all 1's the output current is full scale less 1LSB, i.e., $I.(1-2^{-n})$.

At this stage it is important to point out that the D/A converter will only function as described if the OUT1 and OUT2 nodes are both at the same potential, and furthermore are at ground (AGND). (Chapter 4 discusses some applications where this restriction does not apply.) The standard method of holding OUT1 and OUT2 at ground potential is to use an external op amp connected as a current to voltage converter as shown in Figure 1.1. The feedback resistor R_{FB} is made equal to R and the maximum output voltage is $-I{\cdot}(1-2^{-n}){\cdot}R_{FB}$ where n is the number of bits.

For the six-bit converter of Figure 1.1 the maximum output voltage is $-(63/64){\cdot}I{\cdot}R_{FB}$. Since the remaining one bit worth of current (i.e., I/64), does not exist in the binary system, it is diverted into the ladder termination resistor. The minus sign in the transfer function arises from the inversion introduced by the op amp as a current-to-voltage converter. In a CMOS DAC the resistive ladder is made of thin-film resistors. The feedback resistor R_{FB} is included on the integrated circuit so that $R_{FB} = R$ as nearly as practically possible. This makes the maximum output voltage equal to $-V_{REF}(1-2^{-n})$. The current steering switches are fabricated as NMOS switches whose on-resistance is low enough to be negligible compared with the R/2R ladder resistors in the circuit. In a typical CMOS D/A converter the voltage drop across the switches is about 10mV for a reference voltage V_{REF} of +10V. Note that the input resistance at the V_{REF} terminal is constant and equal to R; this is known as the input (or characteristic) resistance of the DAC and is generally denoted by R_{DAC}.

1.3 MULTIPLYING PROPERTIES

So far, it has been assumed that the reference voltage V_{REF} is fixed. In fact V_{REF} can be any voltage that does not overstress the resistors. It can be negative, positive, sinusoidal or whatever the user prefers. This leads to the name "Multiplying D/A Converter" because the output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the V_{REF} terminal.

$$V_{OUT} = -D{\cdot}V_{REF}$$

D is the fractional binary value of the digital word applied to the converter. One popular use of the CMOS multiplying D/A converter is as an audio attenuator. The audio signal is applied to the V_{REF} node, the digital input determines the attenuation, and the output voltage is the product of the two. Other types of D/A converter are often termed "multiplying converters" but upon close examination their multiplying capability may be restricted to a limited range of input voltage (V_{REF}). CMOS D/A converters can operate with values of V_{REF} up to $\pm 25V$ (check the data sheet for individual part ratings) even though the supply voltage to the circuit may be only +5 volts. Furthermore, since most of the significant voltage drops in a CMOS D/A converter are across high quality thin-film resistors, the device inherently has low noise and low distortion.

1.4 CODES AND TERMINOLOGY

The terminology used in describing CMOS D/A converters does not conform to any particular standard and as a result the various nodes on the circuit are not always labelled the same way. For the purposes of standardization this text will use the designated pin names V_{REF}, OUT1, OUT2, R_{FB} and AGND as described for the circuit of Figure 1.1. In later applications the actual use of these terminals may not be reflected by their name (for example OUT1 can be used as a reference terminal) but the text will strive to differentiate between the designated pin name and the function for which it is used. Also it is often necessary to connect nodes together on the chip in order to reduce pin count and bring them out as a single pin (AGND and OUT2 are often joined): this connection will be clear in most applications, but for further reference Appendix A1 gives the internal connection for all Analog Devices CMOS Multiplying DACs.

The R-2R ladder which forms the basis of CMOS D/A converters has an inherent binary nature. There are several forms of binary code in use and it is useful to examine the relationship between these codes. Key codes in the various number systems for an eight bit number are shown in Table 1.1. The simple binary and 2's complement coding schemes will be known to anyone conversant with contemporary computer practice. Offset binary coding arises as a result of some very simple applications schemes for CMOS DACs which will be covered later. Note

	Negative Numbers				Positive Numbers			
Decimal Value	−128	−127	−64	−1	0	+1	+64	+127
Analog Output V_{OUT}	$(-V_{REF})$	$-V_{REF}\left(\frac{127}{128}\right)$	$-V_{REF}\left(\frac{64}{128}\right)$	$-V_{REF}\left(\frac{1}{128}\right)$	0V	$+V_{REF}\left(\frac{1}{128}\right)$	$+V_{REF}\left(\frac{64}{128}\right)$	$+V_{REF}\left(\frac{127}{128}\right)$
2's Complement	1000 0000	1000 0001	1100 0000	1111 1111	0000 0000	0000 0001	0100 0000	0111 1111
Offset Binary	0000 0000	0000 0001	0100 0000	0111 1111	1000 0000	1000 0001	1100 0000	1111 1111
Sign-Magnitude	Not Available	1111 1111	1100 0000	1000 0001	1000 0000 or 0000 0000	0000 0001	0100 0000	0111 1111

Table 1.1 Analog Output vs. Digital Input for Popular Binary Coding Systems

that offset binary and 2's complement coding are identical save for an inversion of the sign bit. Sign-magnitude coding is also in quite general use in computers; it gives rise to applications circuits slightly different from those for 2's complement coding. The column headings for Table 1.1 also give the analog output voltage which would result from a typical applications circuit.

In a simple binary application the DAC delivers an output which is expressed as a fraction of V_{REF}. Consequently the maximum output voltage is given by:

$$V_{OUT\,max} = -(1\text{-}2^{-n}).V_{REF}$$

This corresponds to all data bits being set to a "1", and is always one bit weight less than $-V_{REF}$. For example if $V_{REF} = -10V$ for the circuit of Figure 1.1 then one bit weight = $10/2^6 = 10/64 = 156mV$ approx. and the maximum output voltage (10 − 0.156) = 9.844 volts.

1.5 WHOLE NUMBERS, FRACTIONS, AND JUSTIFICATION

Converters are normalized to full scale; the MSB has a weight of 2^{-1}, the next has a weight of 2^{-2} and so on all the way to the nth bit, or LSB, which has a weight of 2^{-n}. The largest possible number, all 1's, is 1LSB short of full scale—unity—which is independent of the number of bits. Thus, for converters, the binary code 1 0 1 0 1 is interpreted as the left-justified fractional binary expression, 0.10101_2; (0.5 + 0.125 + 0.03125) = 0.65625.

Computers tend to use whole-number coding; the LSB has a weight of 1(viz., 2^0), the next has a weight of 2(viz., 2^1), the next a weight of 4(viz. 2^2), and so on all the way to the MSB, with a weight of $2^{(n-1)}$. The largest possible number, all 1's, is 1LSB short of full scale, which is 2^n (a function of the number of bits). Thus the binary code, 1 0 1 0 1, is interpreted by the computer as the right-justified whole number, 10101, equal to $2^4 + 2^2 + 2^0$ – i.e., 21. The DAC, on the other hand, interprets the number as $2^{-1} + 2^{-3} + 2^{-5}$ to produce an output of 21/32, or 0.65625 of full scale.

The two systems are equivalent, as they must be; the former is easier to use when considering individual bits; the latter is easier for computing the decimal value of a binary word.

As a result of this duality, two bit-numbering systems have come into use for converters, one left-justified, the other right-justified:

MSB(Bit 1) Bit 2..Bit 3.....(Bit n)
MSB Bit(n-1) Bit(n-2).....Bit(n-3)....Bit 0

Converters that interface with computer buses use the right-justified bus notation for pin-labelling, DB0 for the LSB to DB(n-1) for the MSB. Many other types (e.g., AD7530, AD7523) use the left-justified notation: MSB, Bit 2, etc... Bit n.